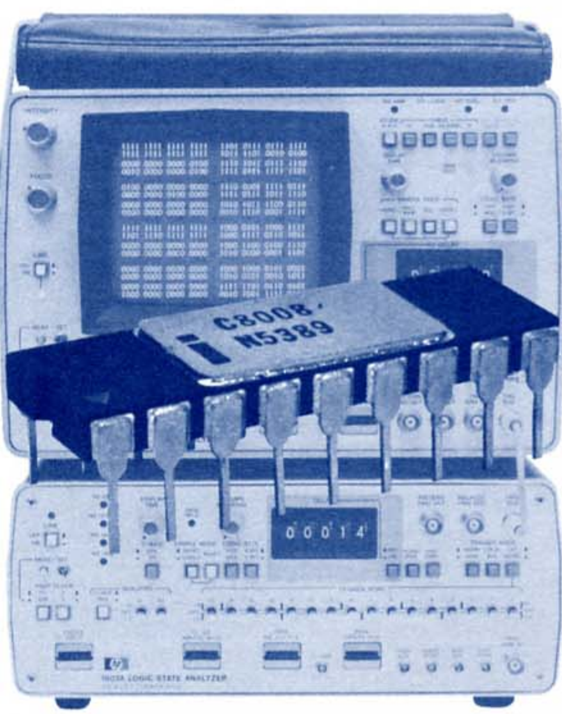
APPLICATION NOTE 167-11
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of Intel 8008 microprocessor systems.



HEWLETT hp PACKARD

1. INTRODUCTION.

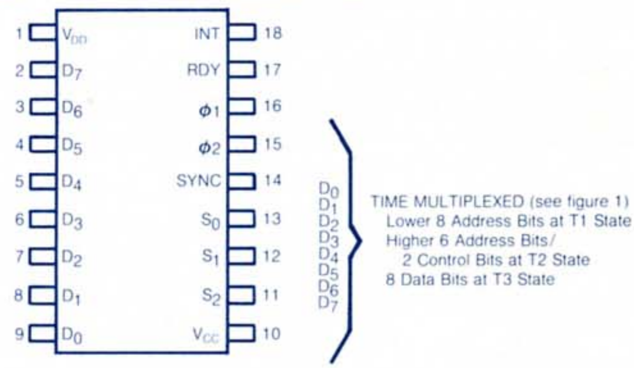
This application note is intended to assist the 8008 microprocessor user in the real-time analysis of his system in both the design and troubleshooting environments. This note demonstrates real-time analysis of program flow and triggering on a specific event, as well as paging techniques.

The 8008 microprocessor, the core of the 8008 microprocessor family, is constructed with PMOS technology and operates from +5-volt and −9-volt power supplies. Features of the microprocessor include an eight-bit address and data bus (D_0 through D_7) that, by time multiplexing, allows control information, 14-bit addresses, and eight-bit data bytes to be transmitted between the CPU and external memory. The 14-bit address permits direct addressing of 16k words of memory.

The microprocessor provides state signals, cycle control signals, and a synchronizing signal to peripheral circuits. These lines are decoded external to the microprocessor to provide the control and timing signals for the microprocessor system.

All microprocessor inputs are TTL compatible and all outputs are low-power TTL compatible. The 8008 microprocessor operates with a 500 kHz clock.

2. PIN ASSIGNMENTS.



SUMMARY OF CONTROL LINES

INT — When interrupt (INT) line is enabled (HIGH), CPU recognizes interrupt request at next instruction fetch cycle.

RDY — HIGH (Logic "1") indicates to CPU that valid memory data is available. LOW (Logic "0") indicates to CPU that valid memory data is not available.

SYNC — Synchronizing signal indicating the start of each machine state.

S_0, S_1, S_2 — State control signals. S_0, S_1, S_2 control use of the data bus and indicate the state of the CPU to peripheral circuitry.

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T11
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

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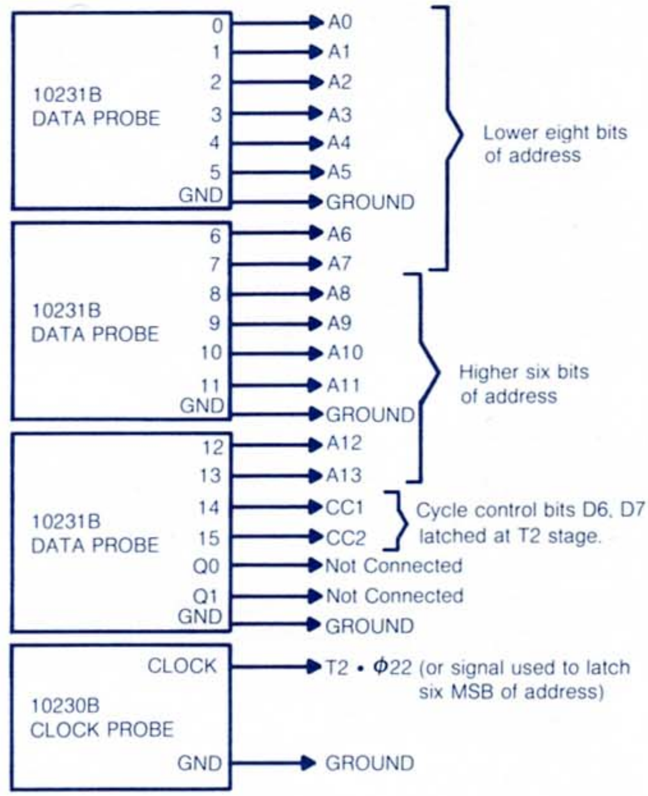
D_6, D_7 (At T2 state) — Cycle control bits designating whether cycle is instruction fetch; data read, data write, or I/O operation.

D_6	D_7	Cycle
0	0	Instruction Fetch Cycle (PCI)
0	1	Data Read (PCR)
1	0	I/O Operation (PCC)
1	1	Data Write (PCW)

3. PROBE CONNECTIONS.

A system that will not "come up" can frequently be debugged by monitoring address flow alone. Since the 8008 14-bit address is time multiplexed, external address latches, such as the Intel 3404 latch, are required in an 8008 system. Connect the Analyzer probes to the output side of the eight LSB address latches and to the input side of the six MSB address latches and the cycle control bit latches. The following Analyzer probe connections provide a display of the activity on the address lines.



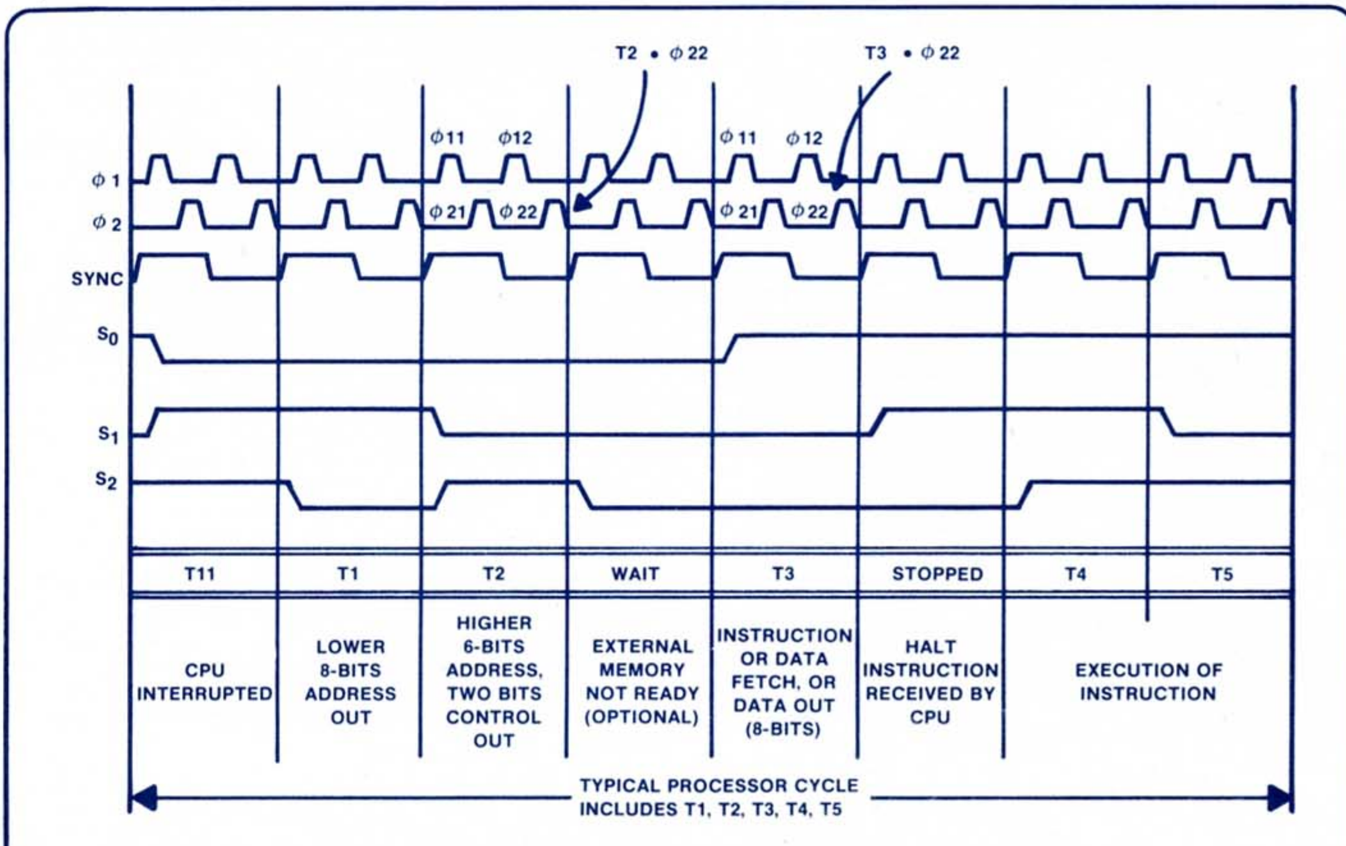


Figure 1. 8008 Timing Diagram

4. SETTING THE CONTROLS.

Turn power on and set Logic State Analyzer controls as follows:

Display Mode	Table A
Sample Mode	REPET [1]
Trigger Mode	
NORM/ARM	NORM
LOCAL/BUS	LOCAL
OFF/WORD	WORD
START DSPL	ON
CLOCK	⎍ [2]
THLD	TTL [3]
All Other Pushbuttons	Out Position
DISPLAY TIME	ccw
COLUMN BLANKING	ccw
QUALIFIER Q1, Q0	OFF
TRIGGER WORD	
Switches	Set to match Address that you wish to trigger on

[1] If program is not looping or cycling through the selected address, select SGL, press RESET, and start your system. The first time the system passes through the trigger point, the display will be generated and stored.

[2] In the system used for this example, the higher six-bit address latches and cycle-code bit latches are clocked on the leading edge (⎍) of T2 • ϕ22. The clocking requirements of your system may vary from the system in this example.

[3] The 8008 output lines are low power TTL compatible as are most address latches. If other logic levels are used, set THLD to Variable and adjust threshold to match your threshold level.

5. DISPLAY INTERPRETATION.

In this illustration, system response to a Call Instruction is considered. The Call Instruction calls a subroutine to check the keyboard for the presence of a stop command and to check system status. Proper operation is confirmed by a comparison between real time state analysis, figure 2a, and the 8008 cross assembler listing output, figure 2b.

The 8008 responds to a Call Instruction in the following manner:

1. Store the content of the program in the push-down address stack.
2. Jump unconditionally to the instruction located in memory location addressed by byte two and byte three of the Call Instruction.
3. Begin execution of subroutine.

Consider the program listing in figure 2b. Observe the three-byte Call Instruction at location 00400. The first byte is the operation code, indicated by 00 in bits 15, 14 columns. The second and third bytes form a double-byte operand (indicated by 01 in bits 15, 14 columns), in this case the address of the first instruction in the subroutine.

Proper operation of the Call Instruction is confirmed by observing that the address immediately following the third byte of the Call Instruction, 00402, is 00572. This means that the microprocessor fetched 172 (lower 8-bits of subroutine address) from location 00401 and 01 (higher six bits of subroutine address) from location 00402).

00 000 101 111 010 ◄ (000 001), (01 111 010)

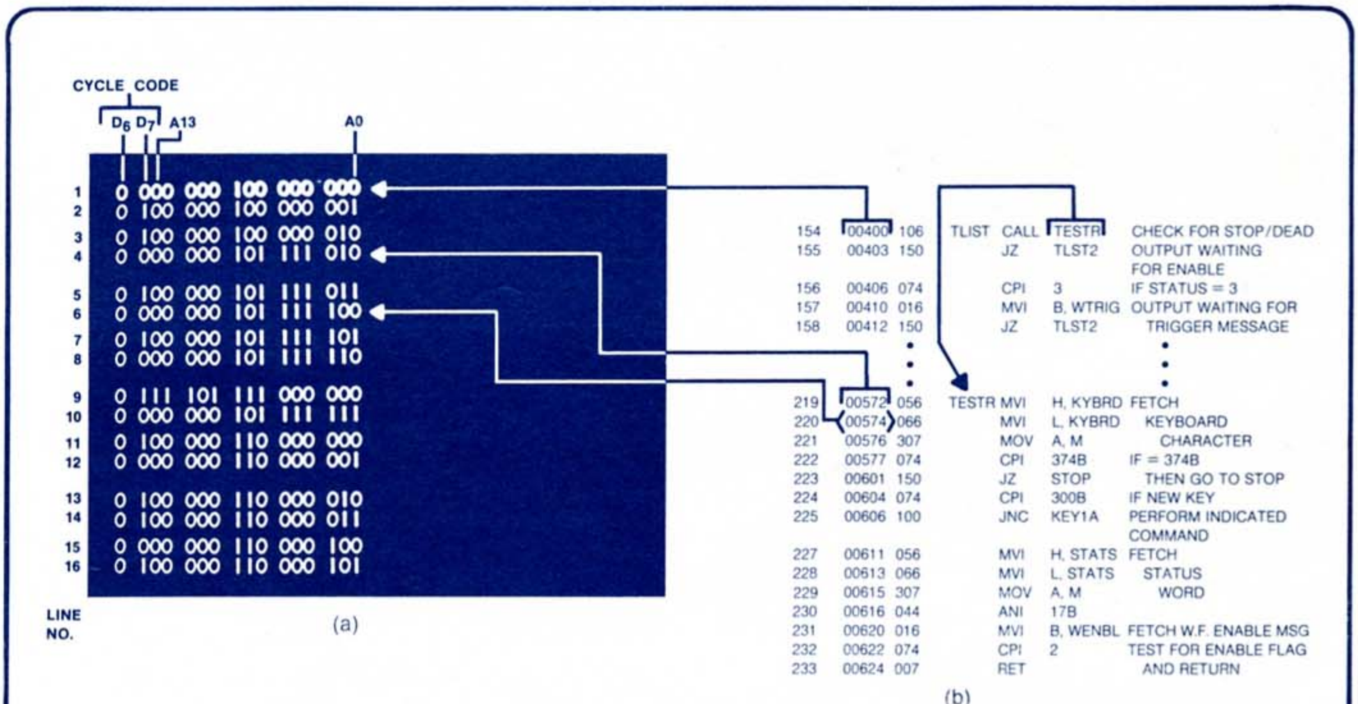


Figure 2. System Response to CALL Instruction

The MVI H, KYBRD and MVI L, KYBRD instructions (Load Keyboard address in H AND L registers) may be confirmed by observing the fourth, fifth, sixth, and seventh lines of the table display photograph. Line 4 is the fetch of the MVI H operation code and line 5 is the fetch of the higher six bits of the keyboard address. Line 6 is the fetch of the MVI L operation code with line 7 being the fetch of the lower eight bits of the keyboard address. Line 8 is the fetch of operation code for MOV A, M and line 9 is the fetch of the keyboard character. In a similar fashion, each instruction in the subroutine may be shown to have been properly executed.

To view addresses following the last displayed address, simply set the Trigger Word switches to match the address displayed in line 16. This address becomes the trigger word in line 1 with the next 15 addresses listed in lines 2 through 16. If you wish to retain the original trigger point, an alternate technique is to use digital delay and set the thumbwheels to 00015 which provides the same display.

6. SELECTIVE STORE.

It may be desirable to not look at every address, but only those corresponding to instruction fetch cycles. We can do this using the Analyzer's Display Qualifier feature. Looking back at the sample program, figure 3b, we see that the subroutine is 14 instructions long with each instruction in the subroutine requiring at least two memory locations. Thus, we cannot view the entire subroutine on the 16-word display in figure 2.

By qualifying the display on the two cycle-control bits, it is possible to look at only addresses corresponding to instruction fetch cycles. We can do this in the following manner:

1. Connect Q1 and Q0 probes to monitor cycle control bits D_6 and D_7.
2. Set DSPLY/TRIG pushbutton to DSPLY.
3. Set Q1 and Q0 switch to LO.

We now obtain the state display shown in figure 3a. Bits 15 and 14 are both zero for every displayed address, indicating each displayed address represents an instruction fetch. Comparing the table display with the program listing reveals that line 1 is the address of the Call Instruction, lines 2 through 15 is the subroutine and line 16 is the return to the main program. Thus, we have an overview of the entire subroutine.

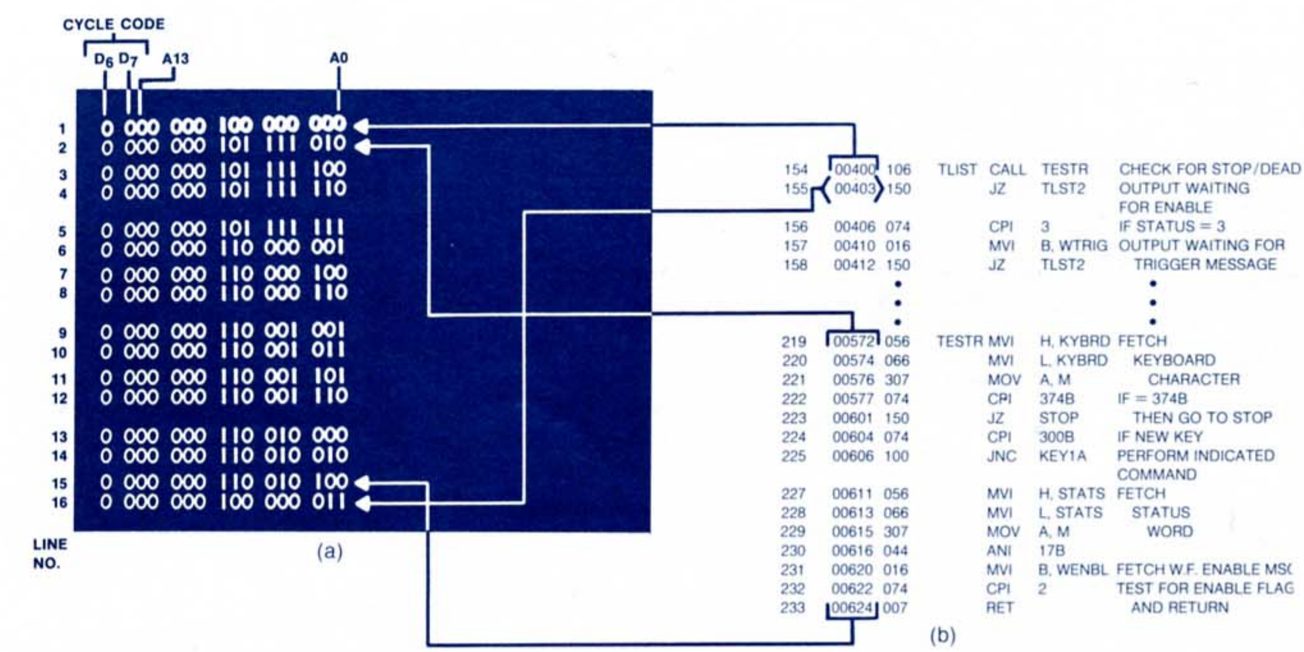


Figure 3. Qualified Display Showing the Ability to Selectively Display Only Desired Addressed Data

7. THE MAP.

If a tabular display is not presented in step 5 and 6, it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to "map" (figure 4). Using the Trigger Word switches move the cursor (circle in photo) to encircle one of the dots on screen. Switch to Expand and make the final positioning of the cursor- the No Trigger light will now go out and switching back to Table A displays the 16 addresses around that point.

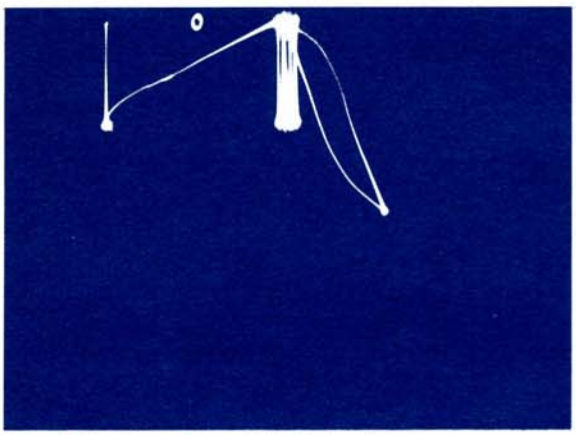


Figure 4. Map Display Shows Entire System Activity

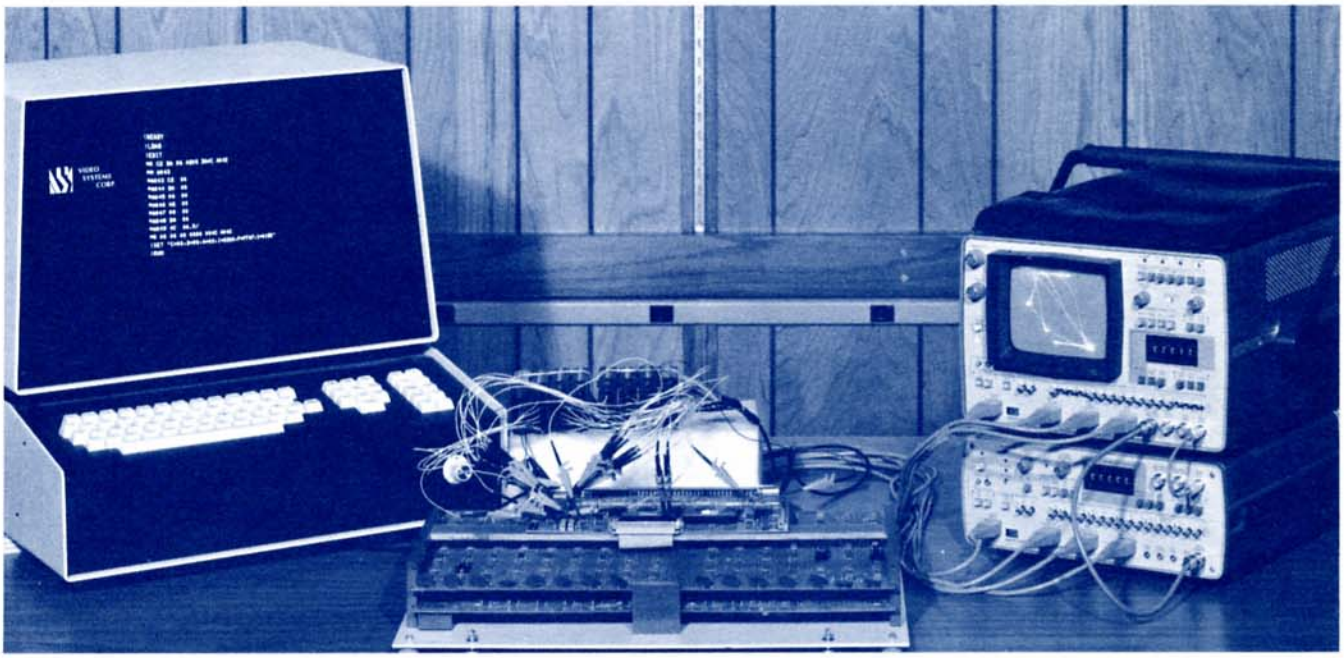
8. VIEWING ADDRESS, DATA, AND CONTROLS.

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data/Control Bus, or other command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A, the display and trigger capability can be expanded to 32-bits wide, allowing the 14 bit address, 8 bits of data, and up to ten other active command signals to be viewed simultaneously. The hook up is easy:

A. Connect data cable between rear panel connectors.
B. Connect trigger bus cable between front panel bus connectors.
C. Set 1600A controls as detailed in part 4 with the following exception: Set display mode to A + B.
D. Set 1607A controls as follows:

Sample Mode	REPET
Trigger Mode	
NORM/ARM	NORM
LOCAL/BUS	BUS
OFF/WORD	OFF
START DSPL	ON
CLOCK	_⌐
THLD	Same as 1600A
DISPLAY TIME	ccw
QUALIFIER Q1/Q0	OFF
TRIGGER WORD	OFF (Don't Care)
All Other Pushbuttons	Out Position



E. Connect 1600A data and clock probes as described in part 3.

F. Connect 1607A data and clock probes as follows:

1. Connect 1607A data inputs 0 through 7 to D_0 through D_7 in order. [4]
2. Connect clock probe to T3•ϕ 22. [5]
3. Connect grounds to appropriate points(s).

G. After a display is on screen, set the 1607A Blanking to display eight columns.

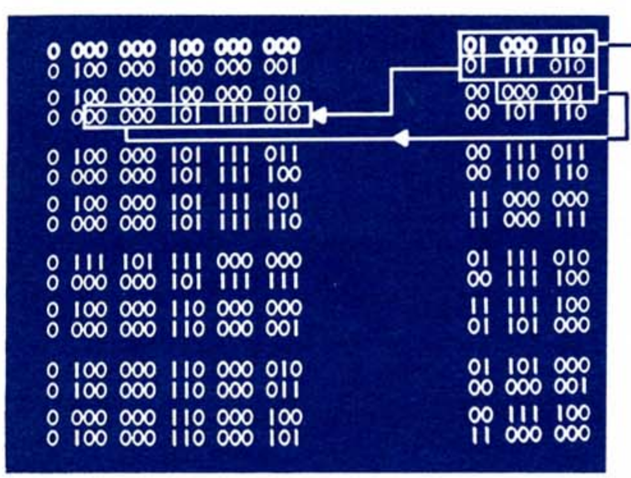
[4] If data bus drivers are employed, connections are made on the driven side of the bus.

[5] If T3 • ϕ22 is not fully decoded in your system the qualifiers can be used to ensure that the 1607A is clocked at the proper time. Connect Q1 probe to SYNC and connect Q0 to T3 (decoded from S_0, S_1, S_2). Connect clock probe to ϕ2. Set Q1 to LO, Q0 to HI, and DSPLY/TRIG to DSPLY. The Model 1607A will now accept data present on the bus only at T3•ϕ22.

9. DISPLAY INTERPRETATION OF ADDRESS AND DATA BUS/CONTROL LINES.

Let's again look at the sample program, figure-5b. By displaying both address and data, it is now possible to confirm exact system operation with respect to the Call Instruction. Looking at line 1 of the state display, figure 5a, observe that bits 15 and 14 of the left-hand table are 00, indicating the 8 bits of displayed data represents an operation code. 01 000 110 is the code for the Call Instruction. The second and third byte of a Call Instruction should be the lower and upper address bits respectively of the subroutine being called. Examination of the address in the fourth line reveals that, indeed, the data bytes of lines 3 and 2 (00 000 001 and 01 111 010) have been combined to form the subroutine address (00 000 101 111 010).

In a similar manner each line of the display can be examined to reveal exact program operation.




```
00400 106   TLIST CALL  TESTR     CHECK FOR STOP/DEAD
00403 150         JZ    TLST2     OUTPUT WAITING
                                  FOR ENABLE
00406 074         CPI   3         IF STATUS = 3
00410 016         MVI   B, WTRIG  OUTPUT WAITING FOR
00412 150         JZ    TLST2       TRIGGER MESSAGE
        •                            •
        •                            •
        •                            •
00572 056   TESTR MVI   H, KYBRD  FETCH
00574 066         MVI   L, KYBRD    KEYBOARD
00576 307         MOV   A, M          CHARACTER
00577 074         CPI   374B      IF = 374B
00601 150         JZ    STOP        THEN GO TO STOP
00604 074         CPI   300B      IF NEW KEY
00606 100         JNC   KEY1A     PERFORM INDICATED
                                  COMMAND
00611 056         MVI   H, STATS  FETCH
00613 066         MVI   L, STATS    STATUS
00615 307         MOV   A, M          WORD
00616 044         ANI   17B
00620 016         MVI   B, WENBL  FETCH W.F. ENABLE MSG
00622 074         CPI   2         TEST FOR ENABLE FLAG
00624 007         RET               AND RETURN
```

Figure 5. System Response to CALL on Address, Data, and Control Lines

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